U.S.S.N. 09/974,584

In The Claims

1. (previously presented) A method for depositing an inter-metal-dielectric (IMD) layer on a semiconductor substrate by plasma chemical vapor deposition (CVD) comprising the steps of:

providing a pre-processed semiconductor substrate;

positioning said semiconductor substrate in a plasma CVD chamber;

heating said semiconductor substrate in said chamber to a temperature between 300°C and 400°C for a length of time sufficient to outgas a surface of said semiconductor substrate; and

conducting a plasma CVD process on said semiconductor substrate and depositing said inter-metal-dielectric layer.

2. (previously presented) A method for depositing an inter-metal-dielectric layer according to claim 1, wherein said semiconductor substrate is preferably heated to a temperature between 350°C and 400°C during said heating step.

3. (previously presented) A method for depositing an inter-metal-dielectric layer according to claim 1, wherein said semiconductor substrate being heated for a time period of at least 30 sec.

4. (previously presented) A method for depositing an inter-metal-dielectric layer according to claim 1, wherein said semiconductor substrate being heated for a time period of at least 1 min.

5. (Original) A method for depositing an inter-metal-dielectric layer according to claim 1, wherein said method prevents said deposited inter-metal-dielectric layer from cracking due to outgassing from said semiconductor substrate.

6. (Original) A method for depositing an inter-metal-dielectric layer according to claim 1, wherein said inter-metal-dielectric (IMD) layer deposited is silicon oxide.

7. (Original) A method for depositing an inter-metal-dielectric layer according to claim 1 further comprising the step of flowing a precursor gas of silane into said plasma CVD chamber for depositing said IMD layer.

8. (Original) A method for depositing an inter-metal-dielectric layer according to claim 1 further comprising the step of flowing precursor gases of silane and nitrous oxide into said plasma CVD chamber for depositing said IMD layer.

9. (original) A method for depositing an inter-metal-dielectric layer according to claim 1, wherein said semiconductor substrate is heated to a temperature of 400°C for 1 min.

10. (Original) A method for depositing an inter-metal-dielectric layer according to claim 1, wherein said heating step and said depositing step are conducted in the same plasma CVD chamber.

11. (previously presented) A method for depositing an oxide layer on a semiconductor wafer comprising the steps of:

positioning a pre-processed semiconductor wafer in a plasma process chamber;

heat-treating said semiconductor wafer at a temperature between 300°C and 400°C for a length of time sufficient to outgas said wafer; and

depositing a silicon oxide layer on said wafer by a plasma enhanced chemical vapor deposition technique.

12. (Original) A method for depositing an oxide layer on a semiconductor wafer according to claim 11 further comprising the step of positioning a pre-processed silicon wafer in said plasma process chamber.

13. (previously presented) A method for depositing an oxide layer on a semiconductor wafer according to claim 11 further comprising the step of heat-treating said semiconductor wafer for a time period of at least 30 sec.

14. (Original) A method for depositing an oxide layer on a semiconductor wafer according to claim 11 further comprising the step of heat-treating said semiconductor wafer at 400°C for 1 min.

15. (Original) A method for depositing an oxide layer on a semiconductor wafer according to claim 11 further comprising the step of evacuating said plasma process chamber prior to said depositing step to a pressure of not higher than 10^{-2} Torr.

16. (Original) A method for depositing an oxide layer on a semiconductor wafer according to claim 11 further comprising the step of cleaning a surface of said semiconductor wafer by a nitrous oxide (N_2O) plasma.

17. (Original) A method for depositing an oxide layer on a semiconductor wafer according to claim 11 further comprising the step of flowing a precursor gas of silane into said plasma process chamber to carry out said deposition process.

18. (Original) A method for depositing an oxide layer on a semiconductor wafer according to claim 11 further comprising the step of flowing precursor gases of silane and nitrous oxide into said plasma process chamber to carry out said deposition process.

19. (Original) A method for depositing an oxide layer on a semiconductor wafer according to claim 11 further comprising the step of depositing said silicon oxide layer as an inter-metal-dielectric layer.

20. (Original) A method for depositing an oxide layer on a semiconductor wafer according to claim 11 further comprising the step of outgassing moisture from said semiconductor wafer during said heat-treating step.